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REMARKS

Claims 1-12 and 25 are currently pending in the present application and are presently under consideration. All pending claims with status identifiers are found at pages 3-6 of this Reply.

Applicants' representative acknowledges with appreciation the Examiner's indication that claims 10-12 would be allowable if recast in independent form to recite all limitations of respective base claims and any intervening claims. However, it is believed such amendments are not necessary in view of the amendments herein and the deficiencies discussed *infra* of the cited art *vis a vis* applicant's claimed invention.

Favorable reconsideration is requested in view of the comments below.

I. Rejection of Claim 1 under 35 U.S.C. §103(a)

Claim 1 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Eriguchi, *et al.* (US 6,113,733) in view of Su (US 6,486,492). Reconsideration and allowance of claim 1 is respectfully requested for at least the following reasons. Eriguchi, *et al.* and Su, individually or in combination, do not teach or suggest all the claim limitations of the subject invention.

In order to establish a prima facie case of obviousness, the teaching or suggestion to make the claim modification *must be found in the cited art*, not based on the applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Furthermore, the mere fact that the reference can be modified does not render the modification obvious unless the cited art also suggests the desirability of the modification. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990).

In particular, and as will be discussed in detail below, neither Eriguchi, *et al.* nor Su teach or suggest *directing... light onto one or more gratings located on at least one portion of the wafer and measuring one or more etching parameters from light reflected from the one or more gratings* as recited in claim 1. Eriguchi, *et al.* teaches a system for detecting defects in a semi-conductor region *via* emitting two light beams - an exciting light and a monitoring light. The exciting light is utilized to excite carriers in the semiconductor region, thereby generating an electric field. The measuring light is

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directed at the same semiconductor region and reflects from the semiconductor region to a capturing mechanism. The reflectance of the monitoring light alters in the presence and absence of the exciting light. Therefore, the exciting light is intermittently emitted, and measurements of reflectance of the monitoring light are taken during instances the exciting light is applied as well as when the exciting light is not applied. A "change rate" is thereafter calculated based upon alteration in reflectance of the monitoring light in the presence and absence of the exciting light (*See* col. 6, lines 8-36). Such alteration of reflectance can thereafter be utilized to determine number of defects in the semiconductor region, thickness of film in the semiconductor region, and depth of damaged layers in the semiconductor region.

In contrast, the present invention as recited in claim 1 directs light upon *one or more gratings*, and thereafter utilizes the reflected light to *measure one or more etching parameters*. The reflected light creates a signature that can be employed to determine various parameters related to an etching process, including but not limited to size of features on a wafer, shape of features on a wafer, location of features on a wafer, chemical properties of a wafer, size of gratings, shape of gratings, location of gratings, size of space between features, shape of space between features, and location of space between features. Thus the present invention as recited in this claim can be employed to measure various critical dimensions related to at least a portion of a wafer directly. Eriguchi, *et al.* cannot be utilized measure numerous features that are measured when employing the invention as recited in claim 1. More particularly, Eriguchi, *et al.* teaches measuring a change rate of reflectance associated with a surface. Such change rate of reflectance, however, gives no indication to size of features, shape of features, dimensions of space between features, *etc.* Furthermore, the present invention as recited in the subject claim *analyzes the etching parameter data by comparing the etching parameter data to stored etching data to generate a feed-forward control data operative to control the at least one etching component*. The present invention can thus be employed to control features measured *via* light reflected from *the one or more gratings*. More particularly, size of features, shape of features, dimensions of space between features, *etc.* can be measured and controlled *via* the present invention as recited in this claim. Eriguchi, *et al.* cannot perform this type of control as Eriguchi, *et al.* cannot

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measure size, shape, and location of features as well as size, shape, and location of spaces between such features.

Su discloses a microscopy system utilized to monitor etching parameters, and then utilizing such monitored parameters as feed-forward information to facilitate control of a semiconductor manufacturing process. The microscopy techniques as taught in Su are expensive, time consuming, and can be destructive when compared to the optical system of the subject invention. Furthermore, like Eriguchi, *et al.*, Su does not teach or suggest *directing light onto one or more gratings located on at least one portion of the wafer and measuring one or more etching parameters from light reflected from the one or more gratings* as recited in claim 1.

In view of at least the above, it is readily apparent that neither Eriguchi, *et al.* nor Su, alone or in combination, teach or suggest the subject invention as recited in independent claim 1. This rejection should be withdrawn.

II. Rejection of Claims 2-6 and 8 under 35 U.S.C. §103(a)

Claims 2-6 and 8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Eriguchi, *et al.* and Su, and further in view of Xu, *et al.* (US 6,483,580). Withdrawal of this rejection is respectfully requested for at least the following reasons. Xu, *et al.* discloses a system for measuring film thickness and optical index of films underneath a diffracting structure utilizing a spectroscopic ellipsometer and an associated spectroscopic scatterometer. However, Xu, *et al.* does not make up for the aforementioned deficiencies of Eriguchi, *et al.* and Su. Therefore, this rejection should be withdrawn.

III. Rejection of Claims 7 and 9 under 35 U.S.C. §103(a)

Claims 7 and 9 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Eriguchi, *et al.*, Su, Xu, *et al.*, and further in view of Ko, *et al.* (US 6,117,791). Withdrawal of this rejection is respectfully requested for at least the following reasons. Claims 7 and 9 depend from independent claim 1. Claim 1 is believed to be in condition for allowance, rendering this rejection moot. Therefore, the subject rejection should be withdrawn.

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IV. Rejection of Claim 25 under 35 U.S.C. §103(a)

Claim 25 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Jahns (US 5,711,843) in view of Su and further in view of Xu. Reconsideration and allowance of this claim is respectfully requested for at least the following reasons. Neither Jahns, Su, nor Xu teaches or suggests combining all elements of the subject claim.

Absent some teaching or suggestion in the prior art to combine elements, it is insufficient to establish obviousness by claiming that the separate elements of the invention existed in the prior art. *Arkie Lures Inc. v. Gene Larew Tackle Inc.*, 43 USPQ2d 1294, 1297 (Fed. Cir. 1997).

More particularly, the cited references do not teach or suggest *partitioning a wafer into... grid blocks and sensing the acceptability of etching in... grid blocks via scatterometry*. Jahns teaches monitoring process environment properties, such as temperature of plasma, gas flow rate, gas pressure, *etc.* (See col. 3 lines 38-44). One or more of such sensed environmental properties are relayed to a process condition monitor, which determines whether any of such properties (or a combination of properties) renders the process defective. Utilizing the invention as disclosed in Jahns, an etching process is labeled as defective based upon parameters within the process chamber, and not based upon parameters of a wafer being processed. Furthermore, the system of Jahns cannot determine portions of a wafer that are defective. Rather, an entire wafer would be deemed defective even in an instance that only a small portion of such wafer was actually defective and could be repaired. Moreover, upon determining that environmental properties are such that etching the wafer is acceptable, etch rates (and various other process parameters) are *estimated* by a classifier based on the environmental properties. Such an arrangement does not facilitate control of etch components particular to grid cells of a wafer. Rather, the processes are controlled for the entire wafer, thus not facilitating achievement of critical dimensions throughout the entirety of the wafer.

Su teaches exposing a wafer to create a focus-exposure matrix, and thereafter examining each matrix cell with a conventional CD-SEM scan. Su does not teach or

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suggest utilizing *scatterometry means for sensing the acceptability of etching in... grid blocks*. Xu discloses utilizing scatterometry techniques to measure one or more parameters of a diffracting structure. Xu does not teach or suggest utilizing *scatterometry means for sensing acceptability of etching in a grid* of a wafer.

The cited prior art references do not exhibit benefits obtained *via* utilizing the invention as recited in the subject claim to control an etching process on a portion of a wafer. Partitioning of the wafer into a grid enables accurate determination of a location in which control of an etching component is required. For example, *via* monitoring individual grid cells, an etching component can be controlled accordingly to facilitate achievement of desirable critical dimensions. Furthermore, the present invention enables *in situ* monitoring and control of an etching component pertaining to a particular grid cell without the expense, complexity, and risk associated with CD-SEM scans. More particularly, CD-SEM scans are known to be expensive, time consuming, and can be destructive. Moreover, etch rates and various other process parameters can be directly measured and controlled, rather than predicting such etch rates based upon processing environment properties such as temperature and gas flow as disclosed in Jahn. There is, however, no teaching or suggestion to utilize *scatterometry means for sensing the acceptability of etching in at least one of the one or more grid blocks* as recited in this claim. In general, the rationale proffered to combine such teachings is to achieve benefits identified in applicants' specification, to overcome problems associated with conventional methods, etc. Applicants respectfully submit that this is an unacceptable and improper basis for a rejection under 35 U.S.C. §103. In essence, the Examiner is basing the rejection on the assertion that it would have been obvious to do something not suggested in the art because so doing would provide advantages stated in Applicants' specification. This sort of rationale has been condemned by the CAFC; see, for example, *Panduit Corp. v. Dennison Manufacturing Co.*, 1 USPQ2d 1593 (Fed. Cir. 1987). More particularly, The Federal Circuit has consistently held that

... 'virtually all [inventions] are combinations of old elements.' Therefore an examiner may often find every element of a claimed invention in the prior art. If identification of each claimed element in the prior art were sufficient to negate patentability, very few patents would ever issue. Furthermore, rejecting patents solely by

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finding prior art corollaries for the claimed elements would permit an examiner to use the claimed invention itself as a blueprint for piecing together elements in the prior art to defeat the patentability of the claimed invention. *Such an approach would be 'an illogical and inappropriate process by which to determine patentability.'* *In re Rouffet*, 149 F.3d 1350, 1357, 47 U.S.P.Q.2d 1453 (Fed. Cir. 1998) (citations omitted).

The Examiner has also indicated that *means for partitioning a wafer into one or more grid blocks* can be interpreted as an entire front surface of a wafer. Applicants' representative respectively disagrees with this rationale. As state previously, the term "partitioning" is defined as "The act or process of dividing something into parts" by The Fourth Edition of The American Heritage Dictionary. Thus, commensurate with the claim, the wafer has to be *partitioned*, and a grid block can thus not be the entire wafer. It is possible, however, to *partition* a wafer so that it includes a single grid block (e.g., a single square within the wafer). Therefore, as described *supra*, a particular portion of a wafer can be monitored, corrected, or deemed defective without requiring an entire wafer to be defective. Furthermore, Fig. 7 and the accompanying text clearly illustrate that a grid block should not be interpreted as an entire front portion of a wafer.

The specification acts as a dictionary when it expressly defines terms used in the claims or when it defines terms by implication. Where the patentee has clearly defined a claim term, that definition usually is dispositive; it is the single best guide to the meaning of a disputed term. *Gutman, Inc. v. Kopyake Enters.*, 302 F.3d 1352 (Fed. Cir. 2002) (citations omitted) (emphasis added).

Fig. 7 clearly shows that a grid block is not an entirety of a wafer, but that if desired a wafer could comprise a single grid block. The common definition of "partitioning" together with illustrations given in Fig. 7 make it abundantly clear that a grid block cannot be interpreted as an entire front surface of a wafer.

In view of the foregoing, it is respectfully submitted that no teaching or suggestion to combine Jahn, Su, and Xu exists in the cited references. This rejection should be withdrawn.

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V. Conclusion

The present application is believed to be condition for allowance in view of the above comments and amendments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063.

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicants' undersigned representative at the telephone number listed below.

Respectfully submitted,

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